Notice of Allowability	Application No. 10/604,587	Applicant(s) CHANG, CHING-YU	
	Examiner Pamela E Perkins	Art Unit 2822	

-- Th MAILING DATE of this communication appears on th cov r sheet with the correspondenc address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiativ of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 12 May 2004*.

2. ☒ The allowed claim(s) is/are *1-9 and 15-24*.

3. ☒ The drawings filed on *31 July 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachm nt(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the amendment on 12 May 2004. Claims 1-24 are pending; claims 10-14 have been withdrawn from consideration.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Cancel claims 10-14.

Allowable Subject Matter

Claims 1-9 and 15-24 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of fabricating a non-volatile memory, where a longitudinal strip of stacked layer is formed over a substrate, wherein the longitudinal strip is a stack that includes a gate dielectric layer, a conductive layer and a cap layer; forming a buried bit line in the substrate on each side of the longitudinal strip; patterning the longitudinal strip to form a plurality of stacked blocks; forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks;

removing the cap layers of some of the stacked blocks to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks; and forming a word line over the dielectric layer and filling the first openings to connect the portion of the conductive layer exposed by the first opening of the stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layers of the stacked blocks are in a second data state.

For example, Chang (6,541,828) discloses a method of fabricating a non-volatile memory where a longitudinal strip stacked layer is formed over a substrate; forming a buried bit line in the substrate on each side of the longitudinal strip; patterning the longitudinal strip to form a plurality of stacked blocks; forming a dielectric layer over the substrate; forming a word line over the dielectric layer. Chang further discloses forming the buried bit line using ion implantation with the longitudinal strip as a mask. However, Chang does not disclose, anticipate, teach, or suggest the longitudinal strip is a stack that includes a gate dielectric layer, a conductive layer and a cap layer; forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks; removing the cap layers of some of the stacked blocks to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks; and forming a word line over the dielectric layer and filling the first openings to connect the portion of the conductive layer exposed by the first opening of the stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding

memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layers of the stacked blocks are in a second data state.

Li et al. (6,545,310) disclose a method of fabricating a non-volatile memory where a longitudinal strip stacked layer is formed over a substrate and forming a word line over the substrate to connect blocks on the same row serially. However, Li et al. do not disclose, anticipate, teach or suggest forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks; removing the cap layers of some of the stacked blocks to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks; and forming a word line over the dielectric layer and filling the first openings to connect the portion of the conductive layer exposed by the first opening of the stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layers of the stacked blocks are in a second data state.

The prior art made of record in this action does not anticipate, teach, or suggest a method of fabricating a non-volatile memory, where a longitudinal strip of stacked layer is formed over a substrate, wherein the longitudinal strip is a stack that includes a gate dielectric layer, a conductive layer and a cap layer; forming a buried bit line in the substrate on each side of the longitudinal strip; patterning the longitudinal strip to form a plurality of stacked blocks; forming a dielectric layer over the substrate, wherein the

dielectric layer exposes the cap layers of the stacked blocks; removing the cap layers of some of the stacked blocks to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks; and forming a word line over the dielectric layer and filling the first openings to connect the portion of the conductive layer exposed by the first opening of the stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layers of the stacked blocks are in a second data state.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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